太欣半導體股份有限公司
SYNTEK SEMICONDUCTOR CO., LTD.

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USB 2.0 DSC/DV Camera controller

STK2265

Product Brief

Version 0.91
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Revision History

Rev.	Date	Author	Description
0.9	2009.11.11	James	First draft
0.91	2009.11.12	James	Correct sensor IF and DRAM size
0.92	2010.09.21	James	Add HDMI IF

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STK2265 Digital Camera Controller

1. Product Overview

STK2265 is a high integration Digital Video Recorder and Digital Still Camera controller. The STK2265 features high quality image processor coupled with high-speed bus and video compression engine delivering excellent quality video recording and playback (HD 720p size 1280x720 at 30 fps). Innovative image processing architecture reduces memory size requirements in both DVR and DSC mode allowing operation with single 8MB SDRAM (4x16 PC133)

Sensor interface module accepts 10 bit data delivered by modern CMOS CCD sensors preserving details in shadows and delivering perfect images even for high dynamic range scenes. We proprietary auto white balance and auto exposure algorithms utilize the statistical data analysis to deliver the precise and pleasing colors. Integrated microphone amplifier, AGC and audio codec reduce system component count and deliver clear audio recordings at all sound levels. The STK2265 is also capable of storing MJPEG videos and JPEG compressed pictures on most popular non-volatile/volatile memory or mini-storage cards. Storage interface utlizing fast DMA allows direct recording to the storage media and supports all major industry standards. Other auxiliary features such as TFT LCD and OLED panel interface, TV display, audio annotation, recording and playback, programmable user interface logic and power management are all integrated into a single chip.

2. Product Features

High Quality Digital Video Recorder and Digital Still Camera functions
- Support up to 32 Mega pixel CMOS/CCD image sensors at capture mode, 10 bit data
- Support up to 256 Mega pixel JPEG still image.
- Support 640x480 MJPEG AVI up to 60 fps
- Support 1280x720p (HD) MJPEG AVI up to 24 fps
- Support 1280x960 MJPEG AVI up to 20 fps

JPEG Compression/Decompression Engine
- Baseline JPEG with support for YCrCb 4:1:1 and 4:2:2 sampling in three component images
- Loadable quantization table to enhance picture quality and compression ratio
- Thumbnail image generation
- Comply to Exchangeable Image File Format (EXIF 2.2)

Image Enhancement Engine
- Highly pipelined architecture for fast shot to shot performance at high resolutions
- Dynamic and static defective pixel removal
- Proprietary color interpolation filter
- Nonlinear color correction matrix
- Smooth gamma curve
- Programmable color space conversion
- Adjustable luminance curve for brightness and contrast
- False color reduction
- Hue and saturation adjustment
- High ISO noise removal
- Advanced edge enhancement
- Precise digital zooming
- Overlay blending with alpha channel, color keying, and scalar

Sensor Interface
- Seamless interface with most CMOS and CCD Image Sensor chips
- Supports up to 9bit sensor data width
- Support for multiple windowed auto focus (AF), auto white balance (AWB) and auto exposure (AE) statistics collection
- Lens/sensor optical defect correction
- Sensor pixel defect correction
- Long exposure noise removal
- Black level clamping
- Support CCIR601/CCIR656 digital video input

Graphical Accelerator Engine

- Bitmap copy including 1,4, and 8 bit mode.
- Support compressed bitmap
- Arithmetic operations including logic operation and color keying
- Image rotation and mirror

Face Detection Engine

- Acclerataed face and facial expression (smile etc.) detection
- General object detection possible with a change of training set

Audio Processor

- Internal microphone amplifier and 16 bit audio codec (SNR 65dB Mic, 80dB Line IN)
- Support AGC
- Support MS ADPCM audio compression

Embedded 32-bit RISC CPU

- 32-bit RISC CPU
- 4KB Instruction, 4KB Data caches

Embedded Microcontroller

- Turbo8032 compatible micro-controller
- Fast fully associative code cache
- 8KB of zero wait state local SRAM
- Integrated with Keil C arithmetic engine for acceleration of 16 and 32-bit operations

Memory Sub-System

- SDRAM – up to 16MB, 16 bit external bus, 4 banks for reduced page break latency
- Support for degraded SDRAM
- Serial Flash support (SPI interface, 2 and 4-bit fast read, DMA)
- Secure Digital (SD)
- Mulimedia Memory Card 4.0 (incl. 8-bit)

Host Interface

- USB 2.0 High Speed Phy built in
- Video Class, Picture Bridge support
- 2x Bulk IN, 2x Bulk Out, 1x ISO, 2x Interrupt endpoints
- High speed UART (16550 compatible)
- Serial synchronous interface
- Support general 8-bit host interface for external controllers.

LCD Interface
- 256 colors overlay with 4-bit alpha blending channel
- Supports all major TFT LCD (incl. AU, Topoly), CSTN and OLED panels with flexible digital interface (8, 16 and 24 bit)
- Built in TV encoder (NTSC/PAL) and   DAC
- CCIR656 output support
- HDMI interface

General Purpose Input/Output Interface
- 22 general purpose input/output ports for user interface and system control
- PWM generator (5 channels)
- Supports Iris control
- Supports IGBT flash bulb control
- Two wire remote keyboard controller
- Support I2C

Miscellaneous Circuit
- Automatic TV detection comparator
- Battery-low voltage detector (8 levels)
- Real Time Clock
- System bootable from SPI flash, and USB

Power management
- Dynamic power management
- independent module clock frequency setting and gating

Software and Development System
- Supports MS-Windows driver for Win98, Win2000, WinME, WinXP
- TWAIN, WIA driver
- Reference development AP
- Reference development hardware platform

Package
- 128-pin LQFP

3. Block Diagrams:

System Block Diagram
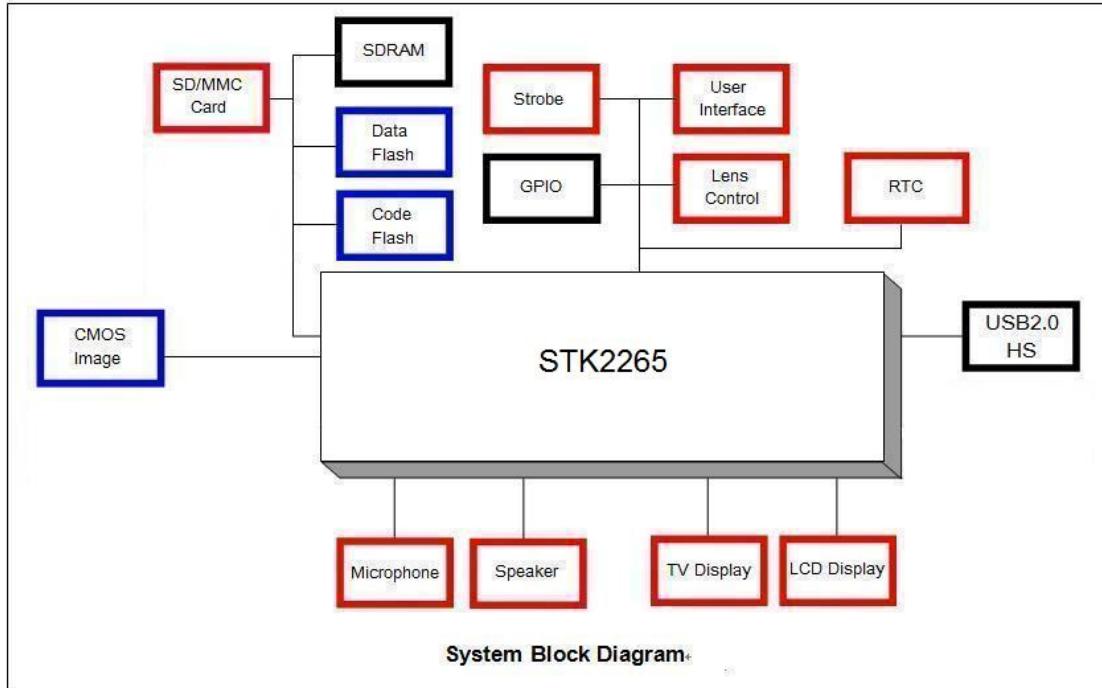
System Block Diagram

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4. Pin Assignment

Top pins (left to right, 128–97):
GPIO0[7] 128, GPIO0[6] 127, GPIO0[5] 126, MD[3] 125, MD[2] 124, MD[1] 123, MD[0] 122, VDD33 121, VSSD 120, GPIO1[7] 119, GPIO1[6] 118, GPIO1[5] 117, GPIO1[4] 116, GPIO0[4] 115, GPIO0[0] 114, VSSD 113, VDD 112, SDDATA3 111, SDDATA2 110, SDDATA1 109, SDDATA0 108, FCFCS1_B 107, FCFCS2_B 106, GPIO0[2] 105, GPIO0[1] 104, RST_B 103, GPIO6[5] 102, GPIO6[4] 101, GPIO6[0] 100, GPIO2[0] 99, GPIO2[5] 98, GPIO2[4] 97

Left pins (top to bottom, 1–32):
1 MD[4]
2 MD[5]
3 MD[6]
4 MD[7]
5 MA[0]
6 VDD33
7 MBE_1
8 MBE_0
9 MA[1]
10 MA[2]
11 MA[3]
12 MA[4]
13 MA[5]
14 MA[6]
15 MBA[0]
16 MBA[1]
17 VDD
18 MCLK
19 MCKE
20 MRAS_B
21 MCAS_B
22 MWE_B
23 MA[7]
24 MA[8]
25 MA[9]
26 VDD33
27 MA[10]
28 MA[11]
29 MD[8]
30 MD[9]
31 MD[10]
32 MD[11]

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Right pins (top to bottom, 96–65):
GPIO2[1] 96
GPIO2[0] 95
VDDA_HP 94
HPOUT_L 93
VCOM_HP 92
VDDA_CODEC 91
VREF_DAC 90
MIC_N 89
MIC_P 88
OSCO_RTC 87
OSCI_RTC 86
RTC_AVDD 85
PLL_AVDD 84
XOUT 83
XIN 82
USB_VS33P 81
DMINUS 80
DPLUS 79
USB_VD33P 78
USB_REXT 77
VCOMM 76
VREST 75
VIDEO_OUT 74
TV_AVDD 73
BATT_IN 72
VDD 71
VDD33 70
GPIO2[2] 69
GPIO2[3] 68
GPIO3[7] 67
LCD_DATA[2] 66
LCD_DATA[3] 65

Bottom pins (left to right, 33–64):
GPIO4[5] 33, GPIO4[6] 34, GPIO4[7] 35, MD[12] 36, MD[13] 37, MD[14] 38, MD[15] 39, VDD33 40, VSSD 41, CD_1 42, CD_2 43, CD_3 44, CD_4 45, CD_5 46, CD_6 47, CD_7 48, VSSD 49, VDD 50, CD_8 51, CD_9 52, CVREF 53, CHREF 54, CCLK 55, GPIO1[0] 56, LCD_CLK 57, LCD_HSYNC 58, LCD_VSYNC 59, LCD_DATA_ENA 60, LCD_DATA[7] 61, LCD_DATA[6] 62, LCD_DATA[5] 63, LCD_DATA[4] 64

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5. Pin List:

Pin	Pand Name	PU/PD	I/O	Commennt
1	md_4	PU	I/O	SDRAM data 4, power on strap 4
2	md_5	PU	I/O	SDRAM data 5, power on strap 5
3	md_6	PU	I/O	SDRAM data 6, power on strap 6
4	md_7	PU	I/O	SDRAM data 7, power on strap 7
5	ma_0		O	SDRAM address 0
6	VDD33		Power	3.3V
7	mbe_1		O	SDRAM byte enable 1
8	mbe_0		O	SDRAM byte enable 0
9	ma_1		O	SDRAM address 1
10	ma_2		O	SDRAM address 2
11	ma_3		O	SDRAM address 3
12	ma_4		O	SDRAM address 4
13	ma_5		O	SDRAM address 5
14	ma_6		O	SDRAM address 6
15	mba_0		O	SDRAM bank address 0
16	mba_1		O	SDRAM bank address 1
17	VDD		Power	1.8V
18	mclk		O	SDRAM CLK
19	mcke	PD	O	SDRAM CLK enable
20	mras_b		O	SDRAM RAS
21	mcas_b		O	SDRAM CAS
22	mwe_b		O	SDRAM WE
23	ma_7		O	SDRAM address 7
24	ma_8		O	SDRAM address 8
25	ma_9		O	SDRAM address 9
26	VDD33		Power	3.3V
27	ma_10		O	SDRAM address 10

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28	ma_11		O	SDRAM address 11
29	md_8	PU	I/O	SDRAM data 8, power on strap 8
30	md_9	PU	I/O	SDRAM data 9, power on strap 9
31	md_10	PU	I/O	SDRAM data 10, power on strap 10
32	md_11	PU	I/O	SDRAM data 11, power on strap 11
33	gpio4_5		I/O	GPIO, 8051 UART1 TX out, SPI SO (data out)
34	gpio4_6		I/O	GPIO, 8051 UART1 RX in, SPI SI (data in), SPI SO1 (2- and 4-bit mode)
35	gpio4_7		I/O	GPIO, SPI SCLK (clk out)
36	md_12	PU	I/O	SDRAM data 12, power on strap 12
37	md_13	PU	I/O	SDRAM data 13, power on strap 13
38	md_14	PU	I/O	SDRAM data 14, power on strap 14
39	md_15	PU	I/O	SDRAM data 15, power on strap 15
40	VDD33		Power	3.3V
41	VSSD		Power	Ground
42	cd_1	PD	I/O	Sensor data in 1, GPIO14_1
43	cd_2	PD	I/O	Sensor data in 2, GPIO14_2
44	cd_3	PD	I/O	Sensor data in 3, GPIO14_3
45	cd_4	PD	I	Sensor data in 4
46	cd_5	PD	I	Sensor data in 5
47	cd_6	PD	I	Sensor data in 6
48	cd_7	PD	I	Sensor data in 7
49	VSSD		Power	Ground
50	VDD		Power	1.8V
51	cd_8	PD	I	Sensor data in 8
52	cd_9	PD	I	Sensor data in 9
53	cvref		I/O	Sensor vsync in, TG vsync out
54	chref		I/O	Sensor hsync in, TG hsync out
55	cclk		I	Sensor clock in
56	gpio1_0	PU	I/O	GPIO, video clock out
57	lcd_clk		I/O	LCD clock out, GPIO7_0, CCIR 656/HDMI clk out
58	lcd_hsync		I/O	LCD hsync out, GPIO7_1

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59	lcd_vsync		I/O	LCD vsync out, GPIO5_0, CCIR 656/HDMI data 9
60	lcd_data_enab		I/O	LCD data en out, GPIO5_1, CCIR 656/HDMI data 1
61	lcd_data7		I/O	LCD data out 7, GPIO5_7, CCIR 656/HDMI data 7
62	lcd_data6		I/O	LCD data out 6, GPIO5_6, CCIR 656/HDMI data 6
63	lcd_data5		I/O	LCD data out 5, GPIO5_5, CCIR 656/HDMI data 5
64	lcd_data4		I/O	LCD data out 4, GPIO5_4, CCIR 656/HDMI data 4
65	lcd_data3		I/O	LCD data out 3, GPIO5_3, CCIR 656/HDMI data 3
66	lcd_data2		I/O	LCD data out 2, GPIO5_2, CCIR 656/HDMI data 2
67	gpio3_7		I/O	GPIO, UART2 TX out, LCD DATA 1 out
68	gpio2_3	PU	I/O	GPIO, SDA (SIF 1)
69	gpio2_2	PU	I/O	GPIO, SCK (SIF 1)
70	VDD33		Power	3.3V
71	VDD		Power	1.8V
72	batt_in		Analog	Battery level detector in
73	tv_avdd		Power	TV DAC 3.3V
74	video_out		Analog	TV DAC video out
75	vrset		Analog	TV DAC bias resistor
76	vcomm		Analog	TV DAC decoupling
77	usb_rext		Analog	USB Phy bias resistor
78	usb_vd33p		Power	USB Phy 3.3V
79	dplus		I/O	USB bus
80	dminus		I/O	USB bus
81	usb_vs33p		Power	USB Phy ground
82	xin		I	USB 12MHz crystal (OSC)
83	xout		O	USB 12MHz crystal (OSC)
84	pll_avdd		Power	PLL 1.8V
85	RTC_AVDD		Power	RTC 1.8V
86	osci_rtc		I	RTL 32768Hz crystal
87	osco_rtc		O	RTL 32768Hz crystal
88	mic_p		Analog	Aux Audio codec microphone in
89	mic_n		Analog	Aux Audio codec microphone in

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90	vref_dac		Analog	Aux Audio codec DAC reference voltage out
91	vdda_codec		Power	Aux Audio codec 3.3V
92	vcom_hp		Analog	Aux Audio codec HP out common voltage
93	hpout_l		Analog	Aux Audio codec HP out
94	vdda_hp		Power	Aux Audio codec HP 3.3V
95	gpio2_0	PU	I/O	GPIO
96	gpio2_1	PU	I/O	GPIO
97	gpio2_4		I/O	GPIO, 8051 UART0 RX in
98	gpio2_5		I/O	GPIO,.8051 UART0 TX out
99	gpio6_0	PU	I/O	GPIO, CCIR 656/HDMI data 0, PWM 0 out
100	gpio6_1	PU	I/O	GPIO, CCIR 656/HDMI data 1, PWM 1 out
101	gpio6_4		I/O	GPIO, CCIR 656/HDMI data 4, PWM 4 out
102	gpio6_5		I/O	GPIO, CCIR 656/HDMI data 5, PWM 5 out
103	rst_b		I	Reset (active low)
104	gpio0_1	PU	I/O	GPIO, Timer 2 out, Audio clk out, TG hsync out, 8051 T2 out
105	gpio0_2	PU	I/O	GPIO, 8051 timer 0 in
106	fcfcs2_b	PU	I/O	CF CS2, GPIO7_7
107	fcfcs1_b	PU	I/O	CF CS1, SD/MMC SDCLK, GPIO14_4
108	sddata0	PU	I/O	SD/MMC data 0
109	sddata1	PU	I/O	SD/MMC data 1
110	sddata2	PU	I/O	SD/MMC data 2, GPIO7_4
111	sddata3	PU	I/O	SD/MMC data 3, GPIO7_5
112	VDD		Power	1.8V
113	VSSD		Power	Ground
114	gpio0_0	PU	I/O	GPIO, internal timer1 output, CLK_TV out, VSYNC out, 8051 T1 out
115	gpio0_4		I/O	GPIO, 8051 T2 input
116	gpio1_4		I/O	GPIO, SPI CS2
117	gpio1_5		I/O	GPIO, SPI CS3
118	gpio1_6	PU	I/O	GPIO
119	gpio1_7		I/O	GPIO
120	VSSD		Power	Ground

121	VDD33		Power	3.3V
122	md_0	PU	I/O	SDRAM data 0, power on strap 0
123	md_1	PU	I/O	SDRAM data 1, power on strap 1
124	md_2	PU	I/O	SDRAM data 2, power on strap 2
125	md_3	PU	I/O	SDRAM data 3, power on strap 3
126	gpio0_5		I/O	GPIO, 8051 timer 2 direction
127	gpio0_6		I/O	GPIO, 8051 INT0
128	gpio0_7		I/O	GPIO, 8051 INT1

6. DC Characteristic:

6.1 Absolute Maximum Rating

Rating	Symbol	Value	Unit
DC supply voltage (IO)	VDD	-0.3 to +4.0	V
Voltage, any pin to ground	V	-0.3 to VDD+0.3	V
DC current drain per pin (excluding VDD , VSS)	I	±10	mA
Operating temperature range	T_A	0 to +70	°C
Storage temperature range	Tstg	-65 to +150	°C

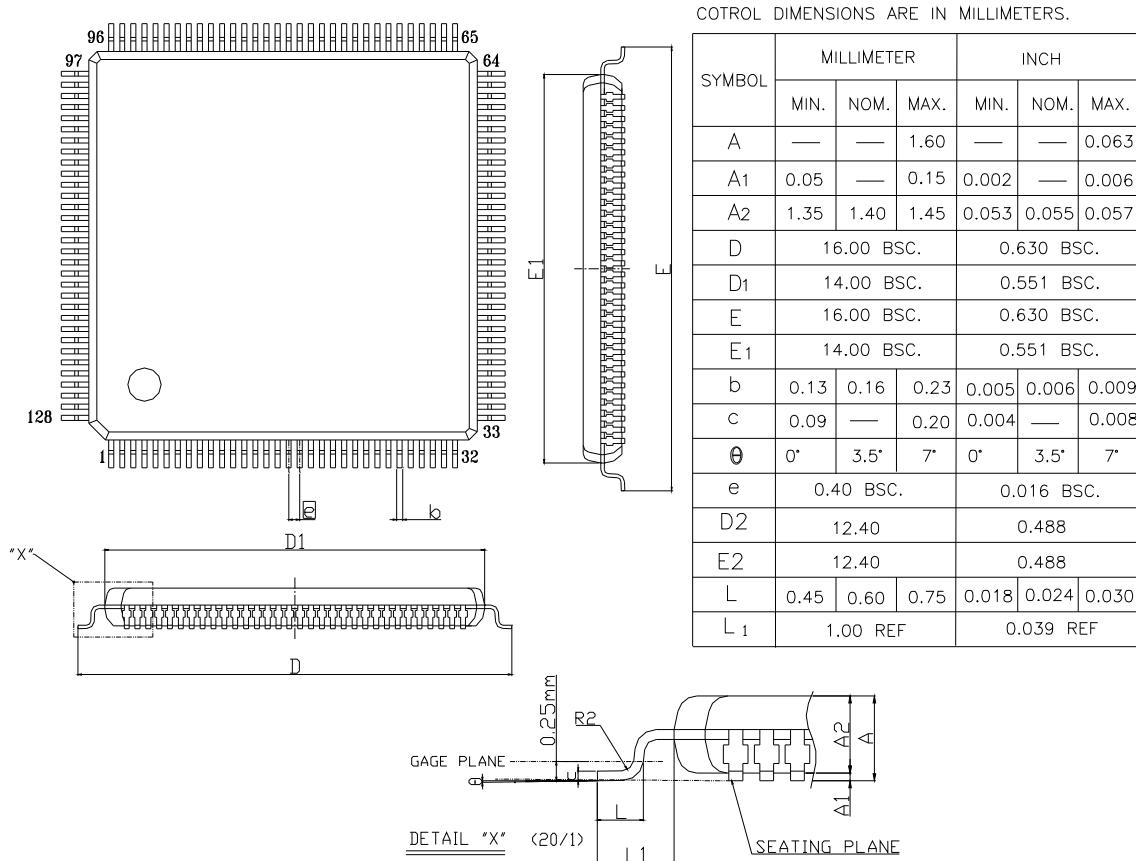### 6.2 Electrical Characteristics (VDD=3.3v, T_A=0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DC supply voltage IO (Vdd to GND)	Vdd	3.00	3.3	3.6	V
DC supply current (@Vdd=3.3v)	Idd		TBD		mA
DC supply voltage core (Vdd to GND)	Vdd_core	1.62	1.8	1.98	V
DC supply current core (@Vdd_core=1.8v)	Idd_core		TBD		MA
Suspend mode current (@Vdd=3.3v)	$I_{Suspend}$		TBD		μA
High level input voltage	V_{IH}	2.0		Vdd+0.3v	V
Low level input voltage	V_{IL}	-0.3		0.8	V
Input current (V_I=Vdd +0.3v or GND)	I_{IN}	-10	1	10	μA
Input capacitance	C_{IN}			10	pF
3-state output leakage current (V_O=Vdd +0.3v or GND)	I_{OZ}	-10	1	10	μA
Output capacitance	C_{OUT}			10	PF
High level output voltage (@Iout=-2ma)	V_{OH}	2.4		Vdd	V
Low level output voltage (@Iout=2ma)	V_{OL}	0		0.4	V
Crystal frequency (at XIN and XOUT pins)	F_{XLT}	5.88	12	24.012	MHz

6.3 USB VP/VM Pins Electrical Characteristics (VDD=3.3v, TA=0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential input sensitivity	V_{DI}	0.2			V
Differential common mode range	V_{CM}	0.8		2.5	V
Output signal crossover voltage	V_{CRS}	1.3		2.0	V
Single ended receiver threshold	V_{SE}	2.0		2.0	V
Static output low (@1.5kΩ pull up to 3.6v)	V_{OL}	0.0		0.3	V
Static output high (@15kΩ pull down to GND)	V_{OH}	2.8		3.6	V
Rise time	T_{FR}	4		20	ns
Fall time	T_{FF}	4		20	ns
Output resistance	Z_{DRV}	28		43	Ω
External D+, D- serial resistor	Rs		24		Ω

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7. Package Drawing:

COTROL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
c	0.09	—	0.20	0.004	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
e	0.40 BSC.			0.016 BSC.		
D2	12.40			0.488		
E2	12.40			0.488		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		